(#48) Real-Time FPGA-Based Audio Processing for Enhanced Acoustic Feedback Suppression

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Abstract

This research aims at proposing a solution to the problem of feedback in audio systems using FPGA technology. Howling or feedback is a kind of acoustic feedback that may lead to deterioration of sound quality, interruption of communication, and even destruction of the used equipment. Based on the parallel processing of FPGA, high-coefficient filters are designed for precise noise reduction. The given research is based on the design and simulation of an adaptive filter that employs the LMS algorithm. MATLAB is used for simulation while Vivado is used for implementation on the FPGA development board and the real-time implementation of the algorithm. The obtained results prove the ability of the LMS algorithm to attenuate the feedback noise with adaptive coefficients and low residual noise. The research provides directions for further study of the more sophisticated adaptive filtering methods and applications for larger audio systems. The concept of using FPGA for audio systems can be promising for improving the performance and the proposed idea can be further developed for real implementation.

Keywords: *howling suppression, fpga, adaptive noise cancellation, least mean square, vivado*

Introduction

Acoustic feedback, or the howling phenomenon, is a cyclic process where amplified voice signals are re-emitted by a speaker, leading to audio degradation, communication disruption, and potential equipment damage [1].

Although there are existing solutions for this problem in the industry, this research introduces the novel integration of FPGA technology. FPGA's capability for parallel processing allows it to handle high-coefficient filters, which can implement highly accurate and efficient noise suppression[2]. This study uses the LMS algorithm as an adaptive filter, which effectively works

with any noise type [3]. The research scope includes designing the algorithm, simulating it using MATLAB and Vivado, and implementing it on an FPGA development board.

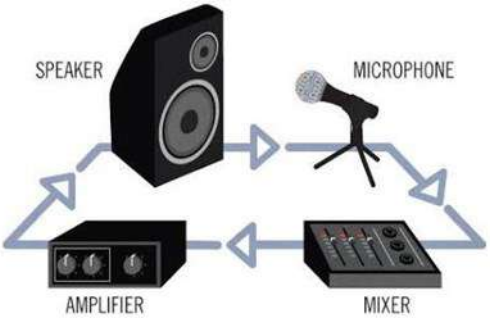

Figure 1: Reason for Feedback Noise *[Image Source: https://m.sohu.com/a/409165410_681125/?pvid=000115_3w_a]*

In the literature review of my research, I have referred to various research papers that are relevant to my topic. These research papers collectively contribute to the understanding and advancement of the relevant topics in my research, providing a solid foundation for my study. Among the notable studies I have explored are,

- "Adaptive Howling Suppressor in an Audio Amplifier System" by W. Loetwassana and R. Punchalard. This research focuses on developing an adaptive howling suppressor using audio amplifier systems [4].
- "An Open Audio Processing Platform with Zync FPGA" by Kevin Vaca. The paper discusses the implementation of an open audio processing platform using Zync FPGA, which offers flexibility and versatility in audio signal processing [5].
- "Study of Howling Suppression Based on FPGA and Wavelet Packet Transform" by Xiaomeng Ma, Zhijun Li, Wei Wang, and Zhiping Chen. This study investigates howling suppression techniques using FPGA and wavelet packet transform, aiming to mitigate the occurrence of howling in audio systems [6].
- "Steady-State Analysis of Continuous Adaptation in Acoustic Feedback Reduction Systems for Hearing-Aids" by Marcio G. Siqueira and Abeer Alwan. The research focuses on the analysis of continuous adaptation algorithms for acoustic feedback reduction in hearing aids, exploring methods to improve feedback cancellation performance [7].

Methodology

The research methodology comprised three key phases. First, the LMS algorithm was mathematically studied and designed for real-time acoustic feedback cancellation. This algorithm employs the steepest descent method to adjust filter coefficients, minimizing the mean square error (MSE) between the desired and actual signals [8]. I developed a block diagram for my application using the LMS algorithm.

In this scenario, the noise in the desired signal and the noisy signal itself serve as the input signals.

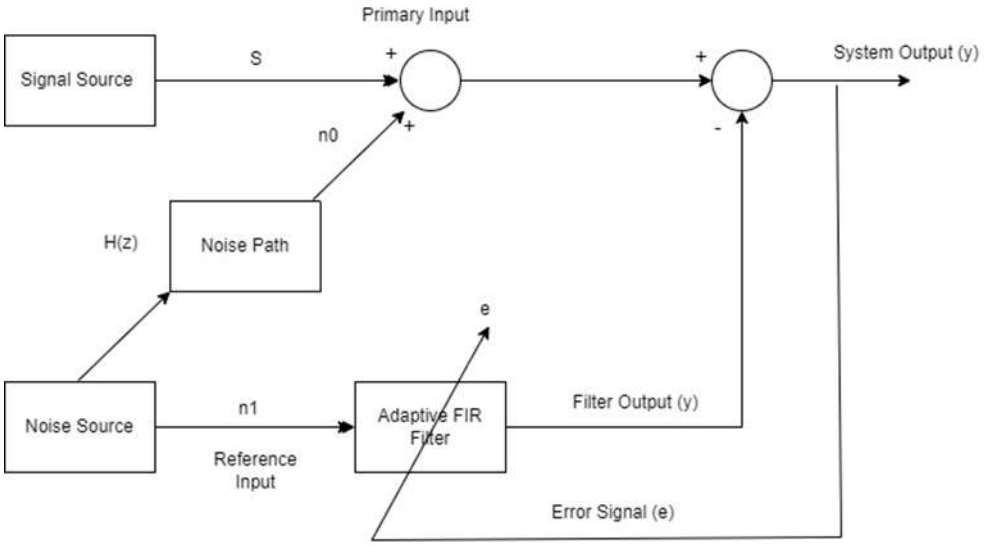

Figure 2: Block Diagram of Feedback suppressor using LMS Algorithm

Second, simulations were conducted using MATLAB to model the LMS adaptive filter while simultaneously developing Verilog code to simulate the LMS algorithm in Vivado. After validating the simulations in both MATLAB and Vivado, the LMS filter in MATLAB was replaced with the function developed in Verilog. This was achieved using Vitis Model Composer to run the Verilog code. The simulation phases included validating the LMS filter performance, observing coefficient changes, and testing noise estimation capabilities.

Finally, the implementation phase involved deploying the algorithm on an FPGA development board, generating bitstreams, and performing real-time testing to refine the algorithm for optimal performance.

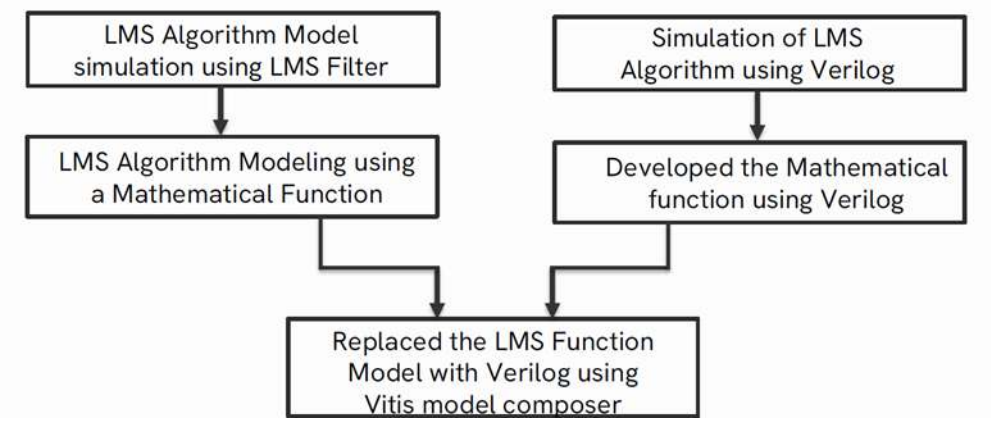

Figure 3: Model Development Process

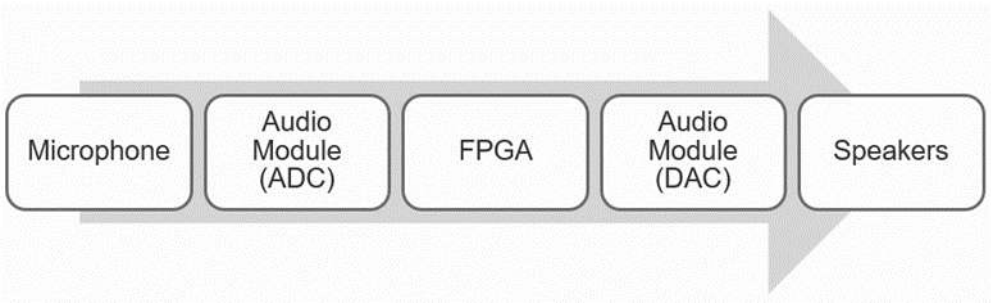

Figure 4: Implementation Plan

Results and Discussion

The simulations confirmed the effectiveness of the LMS algorithm in real-time noise suppression. The MATLAB Simulink models demonstrated the algorithm's ability to adaptively filter out feedback noise, with consistent updates to filter coefficients ensuring minimal residual noise.

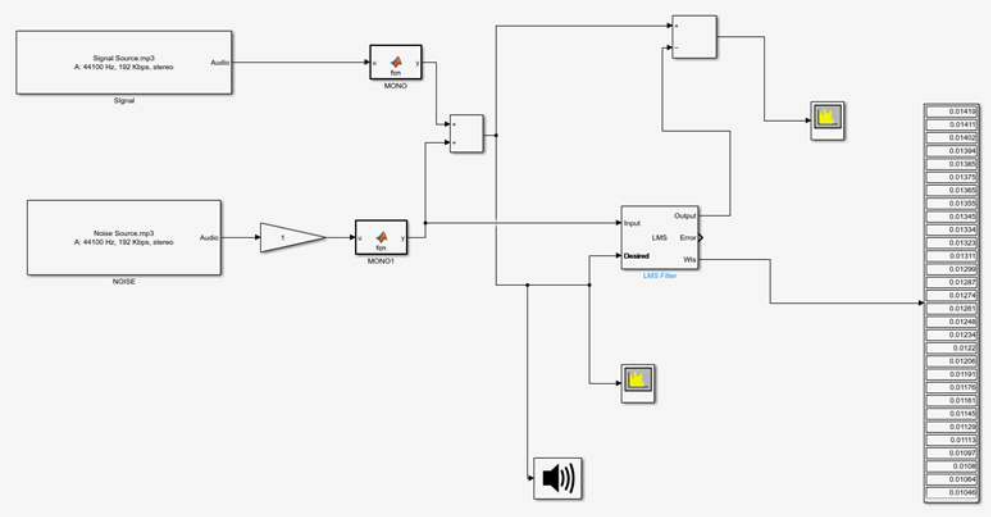

Figure 5: MATLAB Simulink Model using MATLAB Library

This is evident from the comparison of spectra before and after applying the LMS filter.

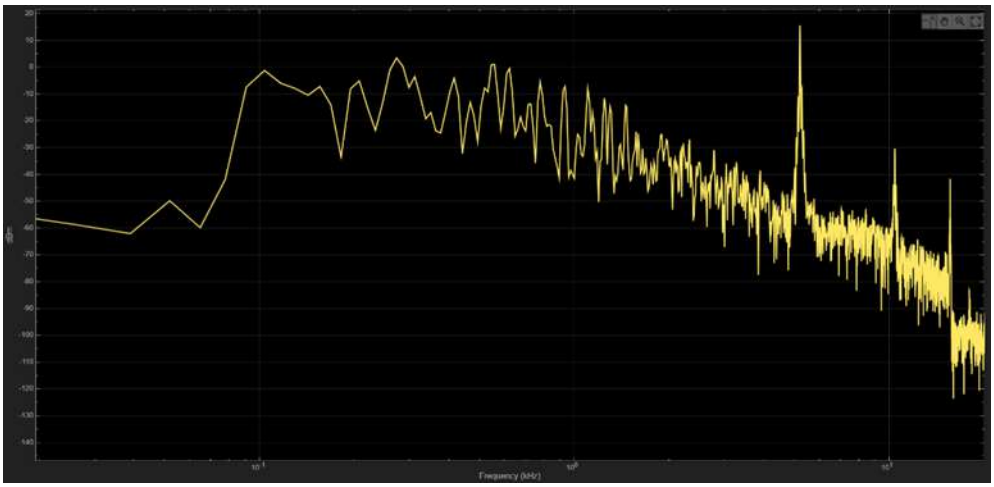

Figure 6: Noisy Signal (Before entering LMS Algorithm)

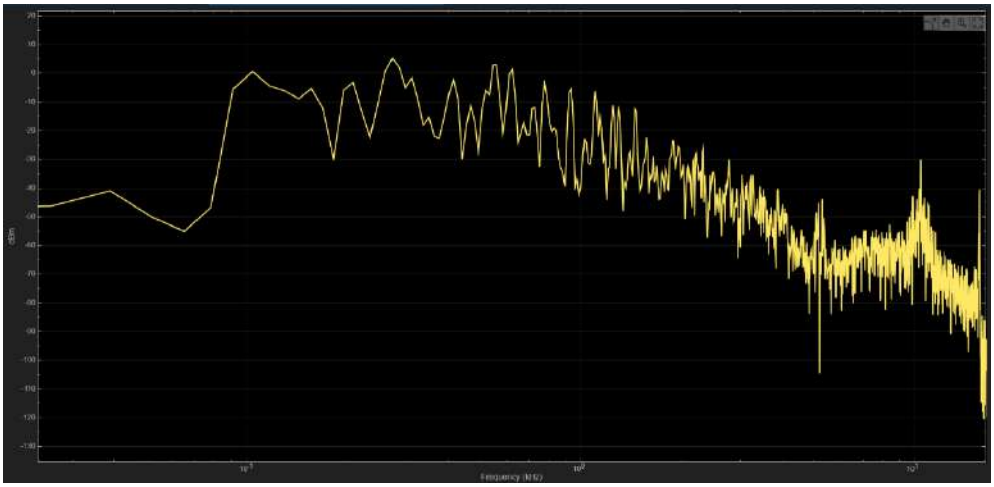

Figure 7: Filtered Signal by LMS algorithm

Additionally, we observed the dynamic changes in filter coefficients as noise passed through the filter, highlighting the adaptive nature of the algorithm.

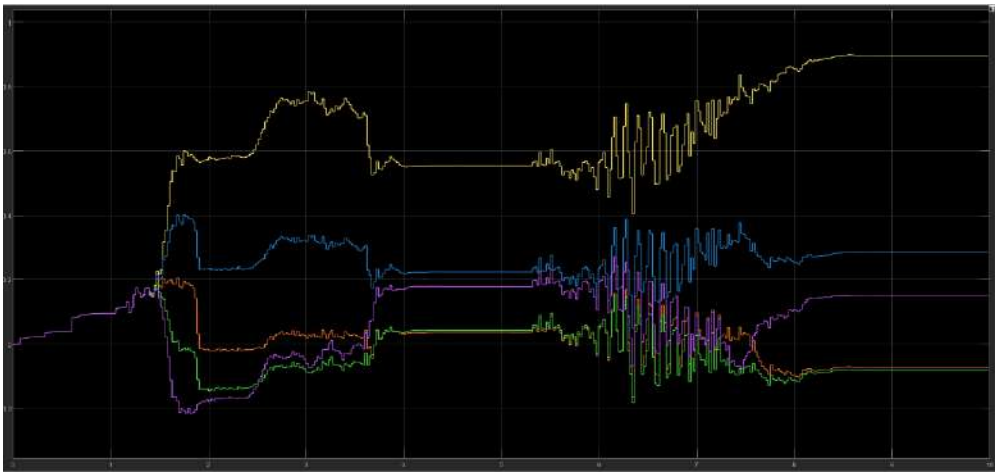

Figure 8: Coefficient Change Over Time

Before developing the Verilog code, a MATLAB function was created to replace the LMS filter, which successfully worked as demonstrated by the function block model. This step ensured that the algorithm's logic was sound before transitioning to hardware implementation.

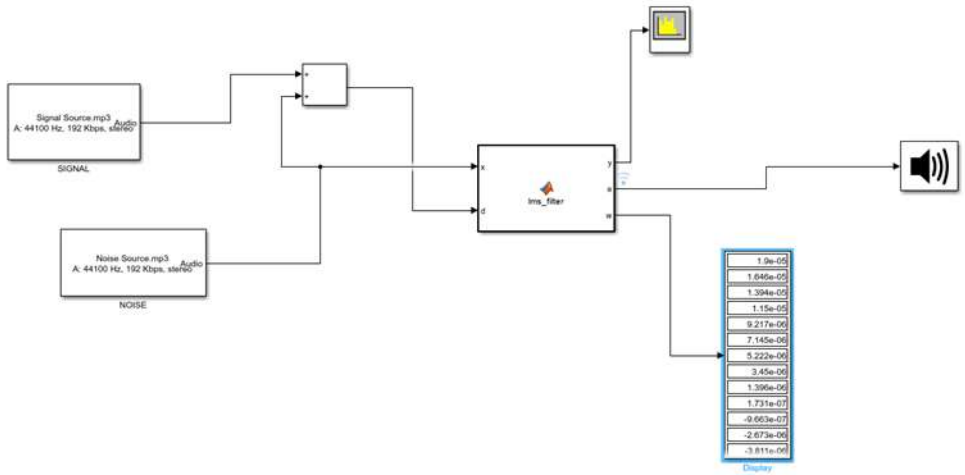

Figure 9: Simulation using Mathematical Function

The transition to Verilog code and subsequent simulation in Vivado maintained the algorithm's integrity, proving its suitability for FPGA implementation. Key observations included the algorithm's computational efficiency and stability in handling unpredictable noise. After developing the Verilog code, it was simulated and verified using a test bench, confirming the algorithm's performance in the FPGA environment.



Figure 10: Behavioural Simulation

Conclusion and Future Work

This research successfully designed and simulated an LMS algorithm for real-time acoustic feedback cancellation, demonstrating its potential for FPGA-based implementation. The findings underscore the algorithm's adaptability, simplicity, and efficiency, making it a viable solution for enhancing audio system performance. The upcoming implementation phase will focus on real-time testing and refinement to ensure robustness in practical applications.

Future research should explore the integration of advanced adaptive filtering techniques to further enhance noise suppression capabilities. Additionally, investigating the scalability of the algorithm for larger and more complex audio systems would be beneficial. Further studies could also address the limitations encountered, such as software compatibility and hardware costs, to make the solution more accessible and cost-effective.

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